

L Number	Hits	Search Text	DB	Time stamp
1	1	("6355555").PN.	USPAT; US-PGPUB	2003/04/25 15:45
2	3	((("5880018") or ("6037664") or ("6010962"))).PN.	USPAT; US-PGPUB	2003/04/25 15:53
3	425	(first adj sacrificial) and (second adj sacrificial)	USPAT; US-PGPUB	2003/04/25 15:54
4	327	((first adj sacrificial) and (second adj sacrificial)) and semiconductor	USPAT; US-PGPUB	2003/04/25 15:54
5	289	((((first adj sacrificial) and (second adj sacrificial)) and semiconductor) and (opening or recess or hole or trench or via))	USPAT; US-PGPUB	2003/04/25 15:56
6	172	((((first adj sacrificial) and (second adj sacrificial)) and semiconductor) and (opening or recess or hole or trench or via)) and @ad<=20000128	USPAT; US-PGPUB	2003/04/25 15:56

US-PAT-NO: 6303486

DOCUMENT-IDENTIFIER: US 6303486 B1

TITLE: Method of fabricating copper-based
semiconductor devices
and an unconstrained
copper anneal

----- KWIC -----

In a dual-damascene copper process flow, according to various embodiments of the present invention, as shown in FIGS. 11-18, a first sacrificial dielectric layer 1120 is formed above the first dielectric layer 1105 and above the first copper structure 1125. A second sacrificial dielectric layer 1130 is formed above the first sacrificial dielectric layer 1120 and above a first etch stop layer (ESL) 1110 (also known as a "hard mask" and typically formed of silicon nitride, Si₃N₄, or SiN, for short). As will be described in more detail below in conjunction with FIG. 12, the first ESL 1110 and a second ESL 1115 define a lower (via) portion of the copper interconnect formed in the dual-damascene copper process flow. The first sacrificial dielectric layer 1120 has the first ESL 1110 formed and patterned thereon, between the first dielectric layer 1105 and the first sacrificial dielectric layer 1120. Similarly, the first sacrificial dielectric layer 1120 has the second ESL 1115 (also typically formed of SiN) formed and patterned thereon, between the first sacrificial dielectric layer 1120 and the second sacrificial dielectric layer 1130. If necessary, the second sacrificial dielectric

layer 1130 may be planarized using chemical-mechanical planarization (CMP).

The first and second sacrificial dielectric layers 1120 and 1130 may be formed from a variety of dielectric materials and one or both may, for example, be an oxide (e.g., Ge oxide), an oxynitride (e.g., GaP oxynitride), silicon dioxide ($\text{SiO}_{\text{sub.}2}$), a nitrogen-bearing oxide (e.g., nitrogen-bearing $\text{SiO}_{\text{sub.}2}$), a nitrogen-doped oxide (e.g., N_{sub.2}-implanted $\text{SiO}_{\text{sub.}2}$), silicon oxynitride ($\text{Si}_{\text{sub.}x}\text{O}_{\text{sub.}y}\text{N}_{\text{sub.}z}$), and the like. The first and second sacrificial dielectric layers 1120 and 1130 may also be formed of any suitable "high dielectric constant" or "high K" material, where K is greater than or equal to about 8, such as titanium oxide ($\text{Ti}_{\text{sub.}x}\text{O}_{\text{sub.}y}$, e.g., $\text{TiO}_{\text{sub.}2}$), tantalum oxide ($\text{Ta}_{\text{sub.}x}\text{O}_{\text{sub.}y}$, e.g., $\text{Ta}_{\text{sub.}2}\text{O}_{\text{sub.}5}$), barium strontium titanate (BST, $\text{BaTiO}_{\text{sub.}3}/\text{SrTiO}_{\text{sub.}3}$), and the like.

The first and second sacrificial dielectric layers 1120 and 1130 may be formed by a variety of known techniques for forming such layers, e.g., chemical vapor deposition (CVD), low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), sputtering, physical vapor deposition (PVD), thermal growing, and the like.

The first and second sacrificial dielectric layers 1120 and 1130 may each have thicknesses in a range of about 1000-2500 .ANG.. In one illustrative embodiment, the first and second sacrificial dielectric layers 1120 and 1130 are each comprised of silicon dioxide ($\text{SiO}_{\text{sub.}2}$) having a thickness of approximately 1000 .ANG., formed by being blanket-deposited by LPCVD process for higher throughput.

As shown in FIG. 12, a metallization pattern is then

formed by using a patterned photomask 1150 (FIGS. 11-12) and photolithography. For example, first and second openings, such as via 1220 and trench 1230, for conductive metal lines, contact holes, via holes, and the like, are etched into the first and second sacrificial dielectric layers 1120 and 1130, respectively (FIG. 12). The first and second openings 1220 and 1230 may be formed by using a variety of known anisotropic etching techniques, such as a reactive ion etching (RIE) process using hydrogen bromide (HBr) and argon (Ar) as the etchant gases, for example. Alternatively, an RIE process with CHF₃ and Ar as the etchant gases may be used, for example. Dry etching may also be used, in various illustrative embodiments.

As shown in FIG. 13, the patterned photomask 1150 is then stripped and a thin barrier metal layer of tantalum (Ta) 1325A and a copper seed layer 1325B are then applied to the entire surface using vapor-phase deposition (FIG. 13). The barrier metal layer of Ta 1325A and the Cu seed layer 1325B blanket-deposit the entire upper surface 1330 of the second sacrificial dielectric layer 1130 as well as the side 1340 and bottom 1350 surfaces of the first and second openings 1220 and 1230, forming a conductive surface 1335, as shown in FIG. 13.

As shown in FIG. 14, this process typically produces a conformal coating of Cu 1440 of substantially constant thickness across the entire conductive surface 1335. As shown in FIG. 15, once a sufficiently thick layer of Cu 1440 has been deposited, the layer of Cu 1440 is planarized using CMP techniques. The planarization using CMP clears all Cu and Ta barrier metal from the entire upper surface 1330 of the second sacrificial dielectric

layer 1130, leaving Cu 1440 only in Cu-filled trench and via 1545, adjacent remaining portions 1525A and 1525B of the one or more barrier metal layers 1325A and copper seed layer 1325B (FIGS. 13 and 14), respectively, as shown in FIG. 15.

As shown in FIG. 16, the first and second sacrificial dielectric layers 1120 and 1130, and the second etch stop layer (ESL) 1115, may be removed by using a wet etch, for example, leaving a Cu-interconnect 1645 remaining. The wet etch stops at the first etch stop layer (ESL) 1110. Dry etching and/or plasma etching may also be used, in various alternative illustrative embodiments. The first and second sacrificial dielectric layers 1120 and 1130, and the second ESL 1115, may also be selectively removed, for example, by stripping with hot phosphoric acid ($H_{sub}3PO_{sub}4$).

By removing the first and second sacrificial dielectric layers 1120 and 1130 before the anneal, the Cu-interconnect 1645 may be formed by annealing the first and second Cu structures 1125 and 1440 together while the second Cu structure 1440 is unconstrained and unstressed by the first and second sacrificial dielectric layers 1120 and 1130. This may further reduce Cu electromigration after the formation of the Cu-interconnect 1645.